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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,321	09/22/2003	Paul C.F. Tong	PS-103	2320

23933 7590 07/15/2005

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EXAMINER	
PATEL, DHARTI HARIDAS	

ART UNIT	PAPER NUMBER
2835	

DATE MAILED: 07/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,321	TONG ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2835	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-18* is/are allowed.

6)☒ Claim(s) *1, 19-20* is/are rejected.

7)☒ Claim(s) *2-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/22/2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that forms the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being unpatentable over Smith, Publication No. 0136126A1. Smith teaches an ESD protection circuit that comprises a power node VDD driven by a power supply; a ground node VSS for coupling to a ground supply; a shunt transistor 31 that conducts current from the power node to the ground node in response to a gate node; a buffer 30c is comprised of PMOS transistor 32 and NMOS transistor 33, that drives the gate node in response to a trigger node; RC circuit 30a having a resistor 39 and a capacitor 38 in series between the power node and the ground node, with the trigger node (RC node) between the resistor and the capacitor; a feedback transistor 34, having a gate driven by the gate node, for conducting current to the trigger node, whereby the shunt transistor 31 conducts current between the power node and the ground node to protect other circuits connected between

the power node and the ground node as disclosed in Col. 4, lines 33-46, 53-67 and Figure 4.

2. ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith, Publication No. 0136126A1, in view of Lin et al., Publication No. 0201457. With respect to claim 19, Smith teaches an ESD protection circuit that comprises a power node VDD; a ground node VSS; a shunt transistor 31 having a channel between the power node and the ground node and a gate connected to a gate node; a stage 30c having a trigger node as an input and the gate node as an output; a feedback transistor 34 having a gate connected to the gate node and a drain connected to the trigger node as disclosed in Col. 4, lines 33-37, 53-67 and Fig. 4. However, Smith does not disclose a resistor connected between the power node and the trigger node and a capacitor connected between the ground node and the trigger node.

Lin et al. teaches a similar technique in his invention of an ESD protection circuit that utilizes a resistor R1 connected between the power node VDD and the

trigger node E; and a capacitor C1 connected between the ground VSS and the trigger node E as disclosed in Col. 4, lines 24-30 and Fig. 3. Therefore it would have been obvious to one of ordinary skill in the art to modify Smith's ESD protection circuit by utilizing the technique taught by Lin et al. for the purpose of having a timing-control circuit.

With respect to claim 20, Smith teaches an ESD protection circuit in which the feedback transistor 34 is a p-channel with a source connected to the power node; the shunt transistor 31 is an n-channel transistor with a drain connected to the power node and a source connected to the ground node; and the stage 30c comprises a p-channel transistor 32 and n-channel transistor 33 in series between the power node and the ground node with drains driving the gate node and gates connected to the trigger node as disclosed in Col. 4, lines 33-37, 53-67 and figure 4.

3. ***Allowable Subject Matter***

Claims 2-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is an examiner's statement of reasons for indicating allowance: Smith teaches an ESD protection circuit which utilizes a feedback transistor that conducts current but it is not in parallel to the resistor. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

4. Claims 12-18 are allowed. The following is an examiner's statement of reasons for indicating allowance: Smith teaches an ESD protection circuit comprising shunt means, buffer means, and feedback means. However, Smith does not disclose time-constant means for initially holding the trigger signal at a first state when a discharge occurs to the first supply line, and for driving the trigger signal to a second state after a timed delay when the discharge occurs. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn Feild can be reached on 571-272-2092. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNN FEILD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800